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| EXAMINER | |
|---|---|
| FAN, CHIEH M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2634 | 16 |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/054,410 | YOUNG ET AL. | |
| | Examiner | Art Unit | |
| | Chieh M Fan | 2634 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16,32-36 and 61-120* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *32-35,61-66,83,84,86,88 and 99-105* is/are allowed.

6)☒ Claim(s) *67-73,75-82,85,87,89-93,98,113,117,118 and 120* is/are rejected.

7)☒ Claim(s) *1-16,36,74,94-97,114-116 and 119* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 1-16, and 36 are objected to because of the following informalities:

Regarding claims 1-16,

a. "a remote xDSL modem" in lines 9-10 of claim 1 should be changed to --- the remote xDSL modem --- since such limitation has been recited in clines 7-8 of claim 1.

b. "said same receive and/or transmit" in line 1 of claim 13 should be changed to --- said receive and/or transmit ---.

Regarding claim 36, "said analog codec and/or" l line 2 should be changed to --- said analog codec ---.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 80, 85, 87 and 89-91 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one

skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 80, and 85, as shown in Fig. 2A of the present application, the bit clock signal (CLOCK) is sent from the analog section (205) to the digital section (230). Therefore, it does not appear that the bit clock signal is generated by the digital control section as claimed. Further, it is not clear how a digital controller can be part of both North Bridge and South Bridge chipsets as claimed.

Regarding claim 87, it is not clear how a digital controller can be incorporated with both North Bridge and South Bridge chipsets as claimed.

Regarding claims 89-91, as shown in Figs. 2A and 2B of the present application, the interfaces 238, 238' and 238" for the USB bus 242, AC-97 bus 243 and PCI bus 241 are not part of the digital link 220. Therefore, the claimed limitations that the digital communications link includes interface for transferring data over a USB based bus or an AC-97 based bus or a PCI bus have no support from the specification.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 67-69, 71-73, 75-79, 92, 93 and 98 are rejected under 35 U.S.C. 102(e) as being anticipated by Timm et al. (U.S. Patent No. 6,055,268, "Timm" hereinafter).

Regarding claim 67, Timm teaches a method of transmitting data over an xDSL digital communications link between a digital controller portion (150 in Fig. 1b) of an xDSL modem and an analog codec portion (170, 172 in Fig. 1b) of the xDSL modem, comprising the steps of:

(a) selecting an xDSL transmission protocol to be used in the xDSL digital communications link (col. 6, lines 54-59; col. 18, lines 33-36; col. 21, lines 26-30 and 33-38); and

(b) configuring a bit clock to accommodate transmission requirements of said selected xDSL transmission protocol (col. 24, lines 7-14, that is, the symbol clock is constant but the bit clock (sample clock) is varied), said bit clock being generated by scaling a separate clock signal useable by the xDSL modem (see DIV in Fig. 1b); and

(c) communicating data between the digital controller portion (150 in Fig. 1b) of the xDSL modem and the analog codec portion (170, 172 in Fig. 1b) of the xDSL modem across the xDSL digital communications link using said bit clock; and

wherein said bit clock is variable to accommodate a plurality of different xDSL transmission protocols (col. 6, lines 54-55).

Regarding claim 68, Timm also teaches a master clock (182 in Fig. 1b).

Regarding claim 69, see col. 9, lines 19-25.

Regarding claim 71, as shown in Fig. 1b, the communication is bi-directional.

Regarding claims 72, 73 and 75, Timm further teaches a word clock ("symbol clock" in Fig. 1b). Timm also teaches transmitting a frame of data and each frame has multiple bits (col. 24, lines 7-15).

Regarding claim 76, see col. 6, lines 54-59.

Regarding claim 77, Timm teaches an A/D converter (172 in Fig. 1b).

Regarding claim 78, Timm teaches FFT (56 in Fig. 4a).

Regarding claim 79, Timm also teaches ATM signals (col. 12, lines 20-24).

Regarding claim 92, Timm teaches a communications protocol for transmitting data over a digital communications link within a computer system between a digital controller (150 in Fig. 1b) and an analog coder/decoder (CODEC) (170, 172 in Fig. 1b), the protocol comprising the steps of:

(a) generating a bit clock (sample clock in Fig. 1b) adapted for data transmission requirements of the digital communications link;

(b) generating a separate frame signal (symbol clock in Fig. 1b) for indicating a boundary for a variable sized data frame transmitting the data between the digital controller and the analog CODEC;

(c) supporting a scaleable data rate in the digital communications link by adjusting a clock rate of said bit clock and/or a size of said variable sized data frame (col. 18, lines 33-36; col. 21, lines 26-30 and 33-38; and col. 24, lines 7-11).

Regarding claim 93, Timm teaches a DSL modem (col. 6, lines 54-59). It is inherent that the clock rate is varies according to the DSL transmission standard.

Regarding claim 98, the word clock signal is used to clock a sample data word from an A/D converter (172 in Fig. 1b) in the CODEC.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 70, 81 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Timm et al. (U.S. Patent No. 6,055,268) in view of the admitted prior art.

Regarding claims 70 and 81, Timm et al. teaches the claimed invention (see the rationale applied to claim 67 above), but does not teach the digital controller is located on the motherboard of a PC and the analog codec is located on a separate board. However, the admitted prior art described in the background section and in Fig. 1 teaches separating the analog and digital portions of a high-speed modem. The digital controller is placed on the motherboard and the analog codec is placed on a card that is physically separated from the motherboard. Such arrangement would keep the analog codec free from the electronic noise from the electronic components on the motherboard. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place the digital controller on the motherboard and

place the analog codec on a card that is physically separated from the motherboard, so as to keep the analog codec free from the electronic noise from the electronic components on the motherboard.

Regarding claim 82, Timm et al. does not particularly teach the bit clock can have a frequency exceeding 35 MHz. However, the bit clock frequency is just a matter of design choice, dictated by system constraint and requirement. The admitted prior art described in the background section teaches an ADSL downstream signal can have a total bit rate of 35.2 Mb/s. Since Timm et al teaches a DSL system, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to choose a bit clock exceeding 35 MHz, so as to clock an ADSL signal.

8. Claims 113, 117, 118 and 120 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Ramachandran (U.S. Patent No. 6,493,326) and Anderson et al. (U.S. Patent No. 5,532,556, "Anderson" hereinafter).

Regarding claim 113, the admitted prior art associated with Figs. 1A and1B of the present application teaches a method of communicating data over a data link (120 in Fig. 1A) connecting a first integrated circuit (130 in Figs. 1A and 1B) located on a first circuit board (131 in Fig. 1B) and a second integrated circuit (110 in Figs. 1A and 1B) located on the a second circuit board (111 in Fig. 1B), the method comprising the steps of:

(a) communicating first transmit data from the first integrated circuit to the second integrated circuit over the data link using a first transmission channel (SDATA-OUT in Fig. 1A); and

(b) communicating first receive data from the second integrated circuit to the first integrated circuit over the data link using a first receive channel (SDATA-IN in Fig. 1A), said first receive channel and said first transmission channel being separate; and

(c) clocking data transmissions in said first transmission channel and/or said first receive channel over the data link using a clock signal (BITCLK in Fig. 1A).

The admitted prior art does not teach the cock signal is a scaleable clock signal, wherein said scaleable clock signal is adjusted for the data link between the first integrated circuit and the second integrated circuit so that the data link uses a scaleable clock rate to support a data transfer rate required for said first transmission channel and/or said first receive channel.

Ramachandran teaches a variable rate vocoder that transmits the audio data at a lower rate to a modem when there is low speech activity (col. 4, lines 2-4). Anderson teaches a protocol for transferring audio data between two audio functional units at multiple rates (see abstract). To support the protocol, an incoming 24.576 MHz clock is divided by 4, 3, or 2 to produce sample bit rates for 24, 32, or 48 KHz, respectively. This bit clock is used for generating serial port clock rates of 6.144, 8.192, or 12.288 MHz.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the clock signal of the admitted prior art with

a scaleable clock signal to support a multiple-rate transferring protocol, and thereby to improve the flexibility.

Regarding claim 117, the bit clock signal (BITCLK in Fig. 1A) is used for both directions.

Regarding claim 118, the data link is set up over a computer bus located on the first circuit board (120 in Fig. 1B).

Regarding claim 120, Anderson further teaches multiplexing the audio data with control information (see claim 2), the control information includes power management signal (col. 9, lines 24-26).

### *Allowable Subject Matter*

9. Claims 32-35, 61-66, 83, 84, 86, 88, and 99-105 are allowed. Claims 1-16 and 36 would be allowable if rewritten to overcome the claim objection. Claims 74, 94-97, 114-116 and 119 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

10. Applicant's arguments filed 1/26/04 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chieh M Fan whose telephone number is (703) 305-0198. The examiner can normally be reached on Monday-Friday 8:00AM-5:30PM, Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (703) 305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Chieh M Fan
Primary Examiner
Art Unit 2634

cmf
April 4, 2004